

PCB 75013 and PCB 75027

10.1 Introduction

The NOTCH FILTER and NOTCH FILTER CONTROL cards are closely coupled, acting as an integrated subsystem. They are therefore treated together under one chapter heading.

10.1.1 Basic Principles of THD Measurement

THD+N (Total Harmonic Distortion and Noise) is a widely used standard for the measurement of the performance of audio equipment. The measurement requires a high purity sinewave to be input to the equipment under test (EUT). Non-linearities in the transfer characteristic of the EUT result in the generation of harmonics of the original signal. These, plus inherent noise of the EUT, are added to the original signal and appear at the output of the EUT. To determine the linearity performance of the EUT, the fundamental frequency is removed and the resulting distortion and noise is measured with respect to the amplitude of the total signal.

Thus to perform this measurement the following processes are required:-

- 1) High purity sinewave generator
- 2) A means of determining the amplitude of the incoming signal (100 % Level)
- 3) A means of removing the original signal (FUNDAMENTAL FILTER)
- 4) A means of detecting the resultant THD+N.
- 5) A means of displaying the ratio of THD+N/100 % LEVEL.

The following paragraphs outline the techniques used in the MJS401D to accomplish these processes.

10.1.2 Sinewave Generator

To allow measurements from any source, there is no connection between the MD404B oscillator output and the measurement system inputs during THD+N measurements.

Any source can therefore be used with no reduction in speed or accuracy. Minimum distortion measurement is determined by the purity of the source.

10.1.3 100 % Level Setting

The system autoranges the appropriate input level to within an 11 dB range, then offsets the gain of the instrument by up to 11 dB to compensate. The result is a gain within 1/8 dB of the ideal value.

For % DIST readings the reference level is set to 1 V = 100 %.
For dB DIST readings it is set to 0 dBu (0.775 V).

The level measurements to control gain setting are made via a precision rectifier within the DOWNSTREAM FILTER PCB (Section 6) whose output is read by a 10 bit A/D convertor on the microcomputer PCB (Section 3). The microcomputer predicts the final level, which is used to set system gain

stages. Minimum settling time for AUTO SET LEVEL is obtained by calibrating the rectifier time constant to match the software cycle time, giving a best match between expected and actual values.

10.1.4 Fundamental Filtering

Removal of the original signal can be accomplished either by a deep and carefully tuned high Q notch filter, or a "brick wall" high pass filter set between the fundamental and second harmonic.

The notch filter has the advantage of being simple and cheap (at least in manual versions), but the disadvantage of allowing noise below the second harmonic to pollute the measured residual. An additional disadvantage is that the notch does not easily track a fundamental which varies in frequency. This frequency variation is often seen from tape and disc playing equipment.

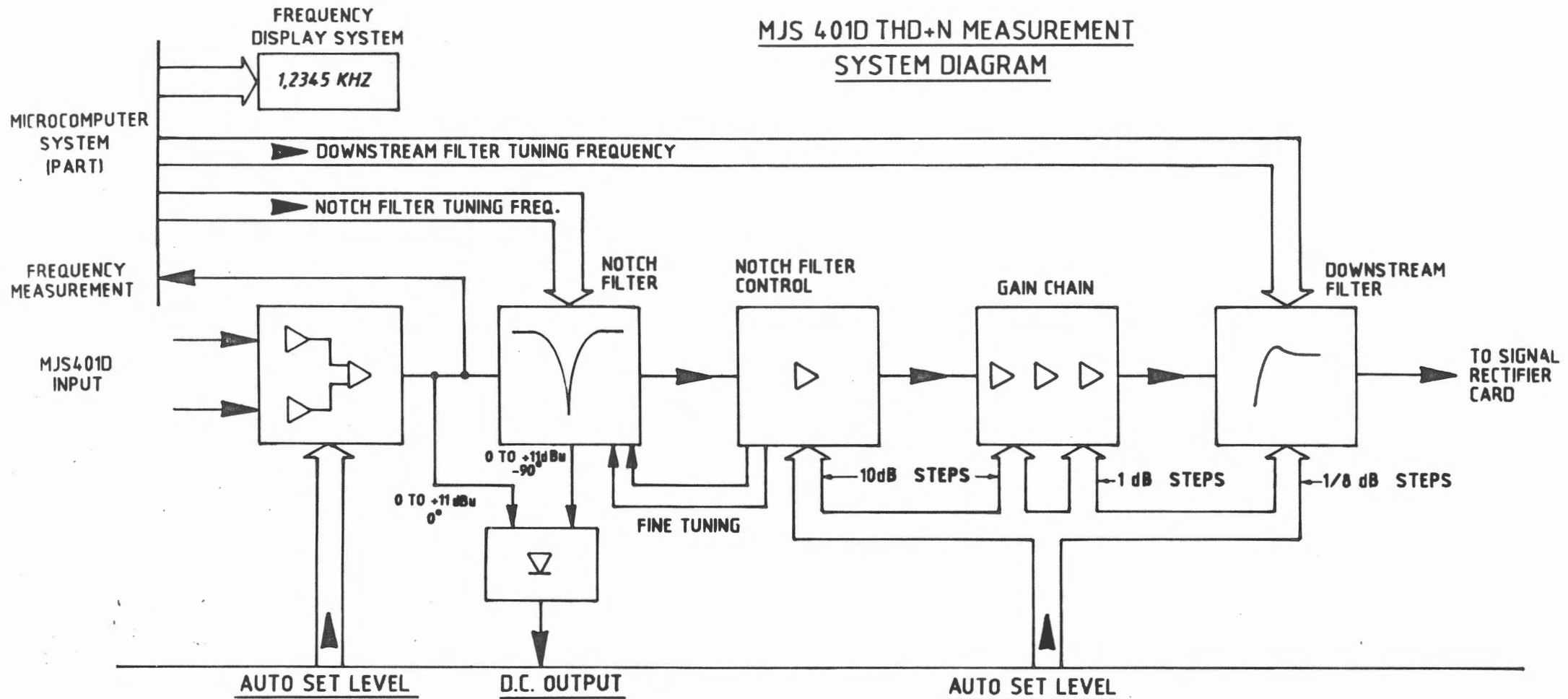
A system based on a high pass filter must have an attenuation rate below cutoff adequate to provide the measurement residual required by the EUT. Since the second harmonic is only 1 octave from the fundamental, and it is undesirable to attenuate the second harmonic, attenuation rates of 100 dB/octave or more are necessary to measure modern equipment. A filter of this complexity is not generally amenable to easy tuning.

The MJS401D uses a fairly low Q notch filter, self nulled to give minimum fundamental output. This filter provides excellent rejection of the fundamental, but attenuates the second harmonic. Being low Q, it is fairly simple and settles quickly. The nature of the filter also makes it tolerant of frequency variation while continuing to attenuate the original signal.

This notch filter is then followed by a high pass filter which is tuned to the second harmonic, having a bump in its response matching the attenuation of the notch filter. This not only corrects the second harmonic, but further attenuates the fundamental and all noise having lower frequency. We call this high pass filter the DOWNSTREAM FILTER in the MJS401D.

Figure 10.1.1 below shows the block diagram of the THD+N Measurement System. The frequency responses of the Notch Filter, Downstream Filter and their combined response are shown in Figure 10.1.2 below.

MJS 401D THD+N MEASUREMENT SYSTEM DIAGRAM



SETS INPUT MODULE GAIN & ATTENUATION SO THAT INPUT TO THE NOTCH FILTER IS IN THE RANGE 0dBu TO +11dBu FOR ANY SIGNAL LEVEL BETWEEN -20dBu AND +40dBu APPLIED TO MJS401D INPUT

INDICATES SIGNAL VOLTAGE TO MICROCOMPUTER VIA ADC

USES ADC VALUE, % DISTORTION SWITCH SETTING AND METER SCALE SETTING TO CONTROL GAIN OF NOTCH FILTER CONTROL, GAIN CHAIN AND DOWNSTREAM FILTER. IN THIS WAY A SIGNAL IS PRESENTED TO THE SIGNAL RECTIFIER, OF A LEVEL CORRECTLY REFERRED TO 100% OR 0dB.

MICROCOMPUTER SYSTEM
(PART)

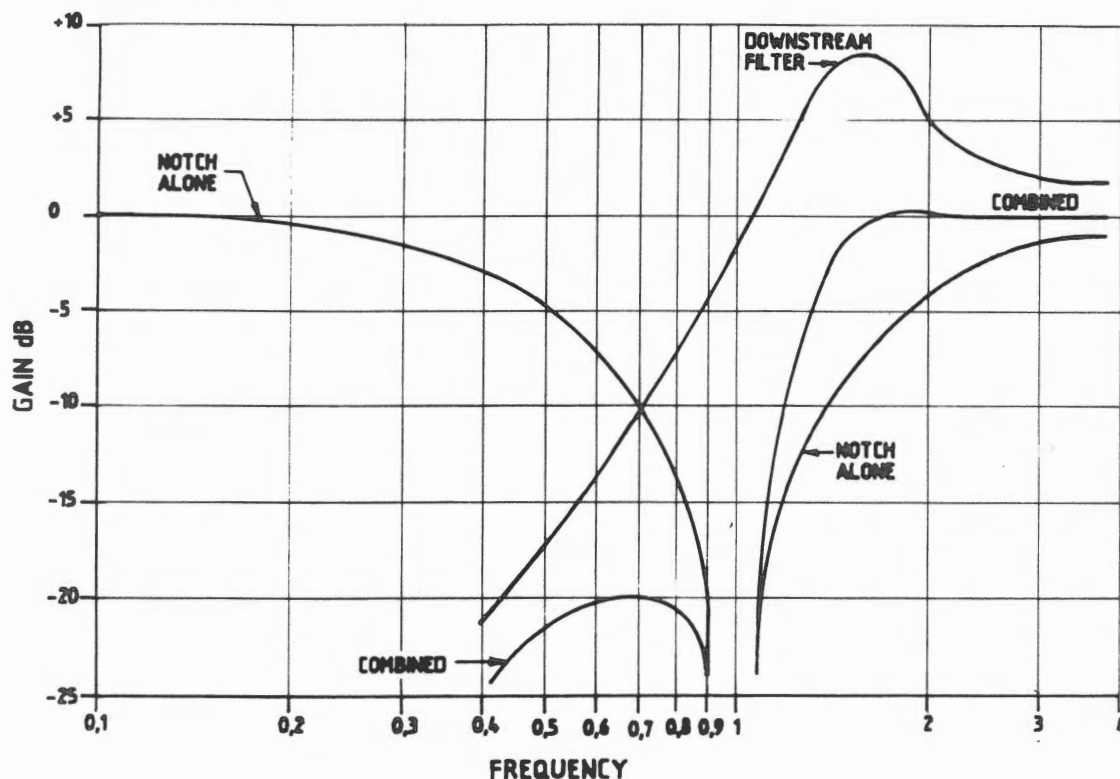


Figure 10.1.2 Frequency Responses, THD+N Measurement System

10.1.5 THD+N Result Measurement

The harmonics plus noise are fed via all the gain adjustment stages on the Gain Chain card, then to a 0 - 7/8 dB stage on the Downstream Filter card. The output from this goes to the Signal Rectifier card (Section 13).

Via front panel control, the required rectifier can be selected. For most purposes the most suitable choice is the True RMS Rectifier since this gives a meaningful result on complex distortion waveforms.

This is then fed to the Meter Driver card (Section 9) which converts the signal for logarithmic (dB) or linear (%) display.

The meter sensitivity is controlled by the % DISTORTION rotary attenuator via the microcomputer system, which controls the gain chain card.

The meter reading is output to the A/D converter on the microcomputer card for access on the option remote control interface.

10.1.6 Ratio Display

The input signal level is adjusted automatically to within an 11 dB range, with a final adjustment of the gain of the residual in 1/8th dB and 1 dB steps. Thus meter readings are inherently referred to 100 % or 0 dB, as selected by the meter scale.

10.1.7 Frequency Measurement/Setting

Different types of equipment require measurement of different frequencies and levels to provide an adequate test of performance. For this reason the MJS401D allows measurement at any frequency from 19 Hz to 21 kHz and at any level from -20 dBu to +40 dBu. Thus it is essential that for automatic measurement both frequency and level are measured prior to giving a THD+N result.

The signal to be measured is input to MJS401D "A" or "B" inputs. This signal, after basic amplitude conditioning in the Input Module, is applied to the frequency measurement system on the microcomputer card. This system measures the frequency 3 - 5 times per second. The frequency is displayed on the instrument display and control outputs are sent to the Notch Filter and Downstream Filter to set basic system tuning.

Tuning is achieved in three decades over the 19 Hz - 21 kHz audio frequency range. The decade switching is effected by changing capacitors (C19, C20, C38, C36) via relay contacts (RLA, RLB).

Tuning within a decade is initially set by the microcomputer selecting the nearest value taps on the two resistor chains via the CMOS analogue switch ICs (IC5, IC6 and IC10, IC15), appropriate to the incoming signal frequency.

Fine tuning is then achieved by using one of the two analogue control loops comprising the two voltage-controlled amplifiers (VCAs) driven from the Notch Filter Control card. Filter balance is achieved by increasing the control voltage to one VCA while decreasing the control voltage to the other VCA by an equal amount. This function is performed by the second analogue control loop on the Notch Filter Control card.

10.2 Circuit description - Notch Filter Card

10.2.1 Notch Filter Operation Overview

Identical circuits are used to control the two frequency-determining RC networks as shown in the notch filter block diagram below.

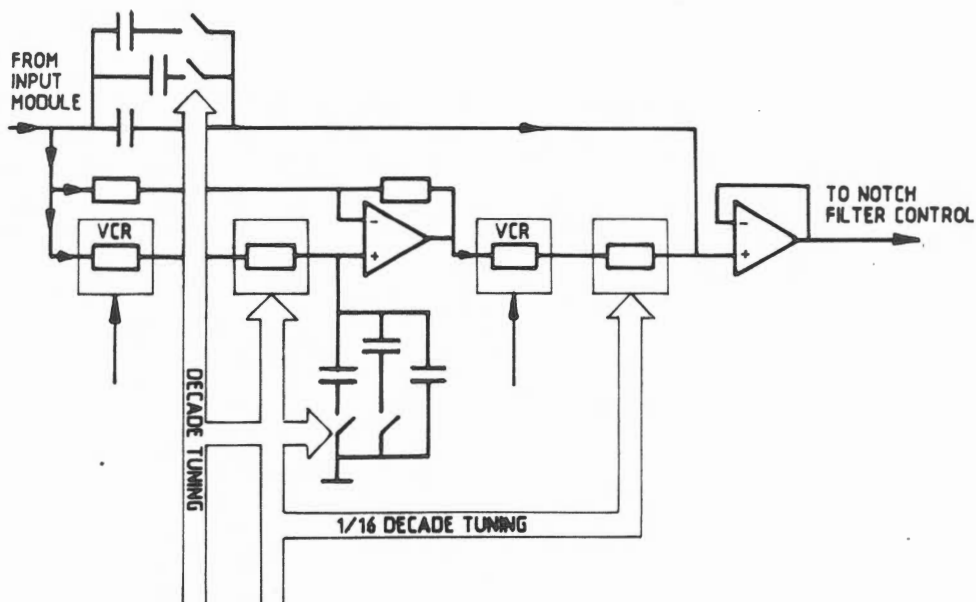


Figure 10.2.3 Notch Filter - Block Diagram

IC9 and its associated components form an all-pass filter. This has a gain of 1 at all frequencies (ideally), but with a phase shift which goes from zero at D.C. to 180° at infinite frequency, passing through -90° at the tuned frequency of the notch filter.

The input signal and the -90° phase shifted signal are fed to another RC filter which feeds IC17, a unity gain buffer. The resulting frequency response at IC17 is a notch, with zero gain at the tuned frequency, and unity gain at D.C. and infinite frequency. Thus the notch filter is able to remove the fundamental frequency of the incoming signal, but to pass its harmonics almost unattenuated.

Each voltage-controlled amplifier has a differential input and single-ended output. Variation of the effective values of the resistive part of the RC networks is achieved by the relevant VCA, which injects an extra current through the resistive part of the RC network proportional to the voltage across the resistor and a function of the control voltage.

This small resistive variable element provides fine tuning for the input chain controlled by voltage VCR1 (0 to -10 V on SKT1/6).

Similarly, VCA2 acts as a voltage-variable resistance across R58, which forms a portion of the output resistance chain of IC9. This provides fine tuning controlled by a d.c. voltage VCR2 (0 to -10 V via SKT3/3) from the notch filter control card.

The coarse tuning for the input resistive chain R18-R51 is provided by a

1-of-16 decoder circuit composed of IC5 and IC6, which select the required resistor by means of four address lines from the microcomputer, via the level shifters, IC18 and IC7.

Simultaneously, the four address lines activate decoder IC10 or IC15, depending on the MSB state, to select the required coarse resistor in the output chain of IC9.

Table 1 shows the nominal centre frequencies for the notch filter for each hexadecimal code on the 4-bit coarse frequency control lines (200 Hz - 2 kHz decade selected).

TABLE 10.2.1 Notch Filter Centre Frequencies

HEX CODE	NOMINAL CENTRE FREQUENCIES (Hz) (VCAs with -4 V approx. at card pins 1/6 and 3/3)
0	200
1	234
2	272
3	316
4	371
5	430
6	504
7	587
8	687
9	797
A	922
B	1.075 k
C	1.267 k
D	1.462 k
E	1.70 k
F	2.00 k

10.2.2 Coarse Tuning

The filter input capacitor C18 permanently in circuit covers the high decade of the frequency range (2 kHz - 20 kHz). At lower signal frequencies, one of two other capacitors is switched across it by contacts of relays RLA, RLB.

Simultaneously, the feedback capacitor C39 is also bridged by one of two other capacitors by contacts of RLA, RLB.

Coarse tuning of the input resistance to IC9 is effected by analogue switch selection to tap into the resistor chain R18, R19, R23-R25, R28-R30, R35-R38, R40, R41, R51, under microcomputer control.

The inputs A, B, C, D on SKT1/3, SKT1/2, SKT1/4, SKT1/5 respectively are active low, normally held at logic +5 V via 22k-ohm pull-up resistors RN1.

IC18 is a non-inverting level shifter which supplies the drivers of analogue switch IC7 and IC16 for coarse output tuning.

The CMOS switches IC5, IC6, IC10 and IC15 are connected to supply rails which are modulated at the same a.c. voltage as would be seen at pin 3 of IC5 or IC6, or pin 3 of IC10 or IC15. This is done to eliminate distortion generated as a result of on-resistance modulation of the switch elements.

The translation of the 4-bit frequency control code from 5 V incoming logic levels at pins 1/3, 1/2, 1/4, 1/5 is accomplished by the non-inverting level shifter IC18 to a 0 V to +18 V logic level, and thence by IC7 and IC16 to a 0 V to +7.5 V level with the a.c. signal voltage superimposed.

Chip selection for the appropriate 1-of-8 decoder is derived from IC7 output pin 7. With the input on SKT1/5 low, output IC7/7 is high and the enable input on IC5/6 is inhibited. However, TR1 is held conductive by the +7.5 V supply across Zener D5 via R47 and diode D4. The collector of TR1 is therefore held low and enable input IC6/6 is activated to select IC6.

Conversely, with the input on SKT1/5 high, output IC7/7 is low and a low enable signal on IC5/6 selects IC5. The low on IC7/7 is also applied via D3 to remove the base drive from TR1. Consequently, TR1 turns off to remove the low enable from IC6/6.

Resistors R42 to R46 are pull-up resistors for the address and enable lines for IC5 and IC6.

The ± 7.5 V supply voltages for IC5 and IC6 are derived via current sources TR2 and TR3 from the -18 V and +18 V rails respectively. The +7.5 V is stabilised by Zener D5 and electrolytic C13; the -7.5 V is stabilised by Zener D6 and C14. The voltage on the mid-point of R55, R57 is equal to that on input pin 3 of the notch filter IC9 (and that on I/O pin 3 of IC5 and IC6). This is applied via voltage follower IC8 to the floating 0 V line. This means that the supply rails to IC5, IC6 are always ± 7.5 V, modulated in respect of the instantaneous voltage on IC8/3, this circuit providing static-to-modulated lines.

The -10 V supply for IC7 (and IC16) pin 4 is derived from potential divider R26, R27 between 0 V and -18 V, decoupled by C11.

10.2.3 Fine Tuning

The differential input section consists of op amps IC4 and IC3. Their outputs are applied to input pins 2 and 7 of a 1537A voltage-controlled attenuator (VCA) IC2, clamped by diodes D1 and D2. The voltage gain of the VCA is controlled by the VCR1 input (0 to -10 V d.c.) from SKT1/6, applied via R2 to pin 8.

The differential outputs on pins 10 and 13 are converted to single ended by op amp IC1. The feedback resistor R7 is chosen to give unity gain; feedback capacitor C1 ensures stability. In effect, the VCA acts as a variable resistance across the low value resistor R6 in the input chain to the notch filter IC9. This provides automatic fine tuning of the overall input resistance value.

Similarly, fine tuning of IC9 output resistance chain is effected by the VCA IC12, controlled by VCR2 on SKT3/3. The differential input amplifiers are IC14 and IC13. The output amplifier IC11 controls the effective resistance across R58 in the output of IC9.

10.3.1 Circuit Description - Notch Filter Control Card

The Notch Filter Control Card provides automatic fine tuning d.c. control voltages (VCR1, VCR2) for the notch filter and selects the post notch filter gain by logic control lines from the microcomputer. In addition it provides a two-line low/high frequency status output to the microcomputer for tuning control sensing purposes. Figure 10.3.1 below shows the block diagram.

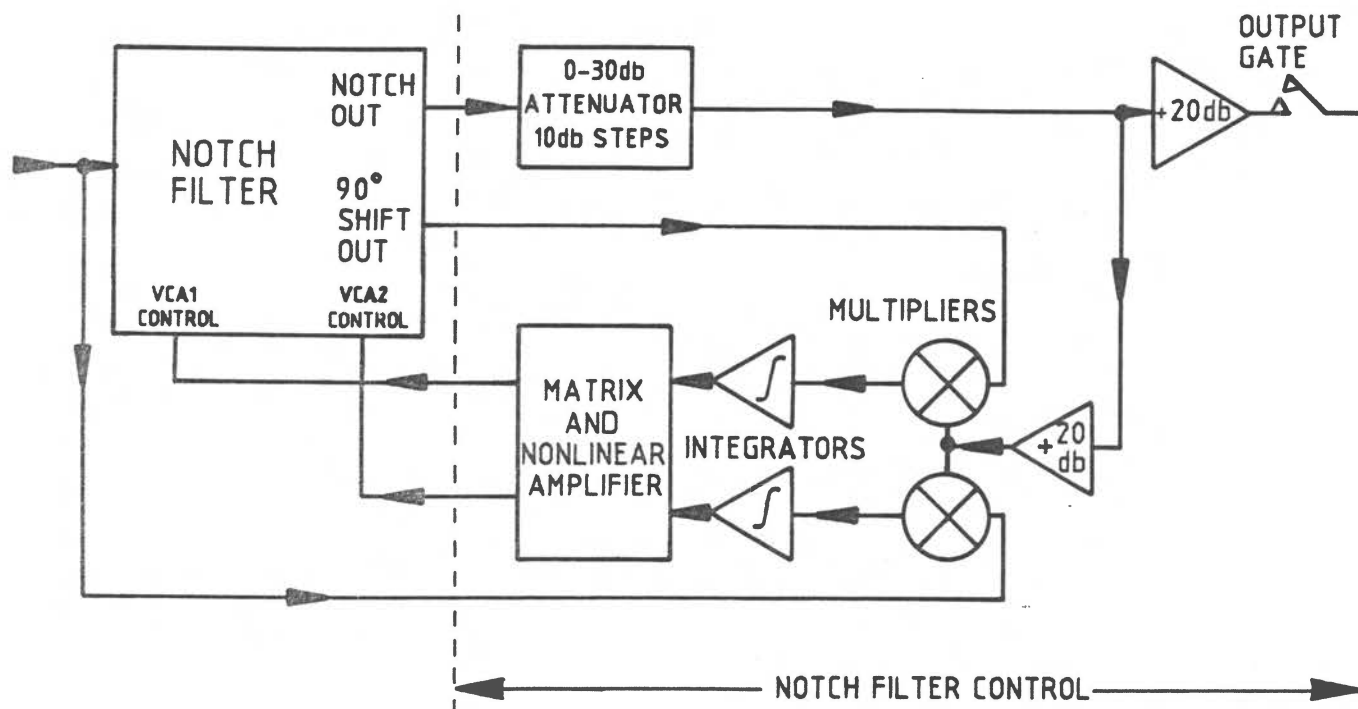


Figure 10.3.1 Notch Filter Control - Block Diagram

The circuit comprises:

- an output error amplifier (IC3) feeding two feedback control loops, each consisting of a synchronous detector (IC2, IC8) driving a differential to single-ended converter and integrator (IC1, IC7) for VCA control.
- a frequency high/low detector (part IC10).
- logic-controlled analogue switches (IC5) to select a post notch-filter attenuator setting.
- T.H.D. output amplifier (IC9) and output gate circuit (RL1).

10.3.2 Output and Error Amplifiers

Output from the notch filter card is applied via SKT3/5 to the top of the attenuator network comprising R39//R40, R41, R44//R46 and R45. The tap selected on the attenuator network by analogue switch IC5 is connected to both IC3 and IC9 inputs.

Output amplifier IC9 feeds the amplified or attenuated THD signal out to the Gain Chain card via the output gate RL1; IC3 feeds the same THD signal to the

synchronous detectors IC2 and IC8, clamped by D10 and D11 in order not to overload IC2 and IC8.

The attenuator network provides between 0 and 30 dB attenuation in four 10 dB steps. Since output amplifier IC9 has 20 dB gain, the input-output gain is as follows:

B (SKT3/6)	A (SKT3/7)	GAIN
L	L	+20 dB
L	H	+10 dB
H	L	0 dB
H	H	-10 dB

The analogue switch IC5 is powered from ± 7.5 V sub-rails derived from the +18 V supplied by R24, D14. The +7.5 V logic level conversions from the 5 V control lines from the microcomputer are provided by IC10 outputs at pins 13 and 14.

The output of IC3 is clamped to the maximum permissible level of ± 4 V for the synchronous detectors IC2 and IC8 by the network R9, D10, R14, R18, D11 and R20.

The +6.2 V sub-rail for IC2 and IC8 carrier inputs is supplied by R47, D15 and decoupled by C15.

10.3.3 Output Gate

For all except a few early models, the output gate consists of RL1.

Early models had a transistor output gate, shown inset in the circuit diagram. When the control input at SKT2/6 is low, TR3 does not conduct. TR2 is biased into conduction by R87, R88 and R89. A voltage greater than the threshold of TR1 is developed across R79. TR1 therefore does not conduct.

When the control input at SK2/6 is high, TR3 conducts sufficient current through R89 to turn off TR2. No voltage is developed across R79, and therefore TR1 turns on, passing the output signal through to SKT2/1.

The transistor output gate must be replaced by a relay if an IMD card is to be used in the MJS401D. Contact your dealer for details.

10.3.4 Tuning and Balance Circuits

The notch filter card requires two separate d.c. control voltages (0 to -10 V) to provide fine tuning and balance to reject the fundamental frequency by more than 100 dB. Fine tuning is achieved by altering the control voltages in the same direction; changing the control voltages in opposite directions effects the balance.

10.3.5 Tuning Detector

The tuning control voltage is derived from the error amplifier IC3 output via the synchronous detector IC8. The lower pair of transistors in IC8 convert IC3 output voltage into a differential current. The polarity of the current difference, as seen between pins 6 and 12 of IC8, is reversed at each zero crossing of the high-level 90° phase-shifted signal applied via IC8/8.

At frequencies much lower than the notch centre frequency (fundamental) the waveform at the synchronous detector differential to single-ended converter (IC7/1) approaches a full-wave rectified negative-going d.c.

At frequencies much higher than the notch filter centre-frequency, the waveform approaches a full-wave positive-going rectified d.c.

However, at the centre-frequency there is no d.c. component in the error voltage waveform at IC7/1, whereupon the correct voltage is present on the tuning integrator output IC7/7.

VR3 is used to adjust the synchronous detector balance to trim out any errors due to resistor tolerances, offsets, etc.

VR4 is used to trim out offset voltage and current at the signal input of IC8, thereby minimising a.c. ripple at IC7/1. In turn, this minimises the tuning control voltage ripple and residual distortion at low frequencies.

10.3.6 Balance detector

The balance control voltage is derived from the error amplifier IC3 output via the synchronous detector IC2. The detailed operation is identical to that described for its 'tuning' counterparts IC8 and IC7.

If the error voltage at IC2 is in phase with the carrier signal applied from the notch filter card input to IC2/8, the resulting signal at IC1/7 looks like a positive-going full-wave rectified waveform.

An error signal out of phase with the carrier results in a negative-going full-wave rectified signal.

However, when the error signal is exactly at $+90^\circ$ with respect to the carrier, no resultant d.c. is present at IC1-7. In turn, this means that no current is flowing in the balance integrator capacitor C6 and the integrator output voltage is correct to ensure optimum balance.

VR2 and VR1 are used to trim IC2 balance for optimum fundamental rejection.

VR1 trims out offset voltage and current for the voltage-current converter pair in IC2 to minimise a.c. ripple on IC1/7. This also reduces the residual distortion at low frequencies caused by control voltage a.c. ripple as described for VR4 in the tuning section.

Zener diodes D12 and D20 across C6 and C24 limit the balance and tuning integrator outputs to between +0.5 V and -13 V.

10.3.7 Tuning and Balance Matrix

This arrangement provides the output control voltages to VCA1 and VCA2 on the notch filter card. For best attenuation of the fundamental, the notch filter control voltages are required to move in the same direction to effect tuning, and in opposite directions to effect balance.

The balance control voltage is applied via R22 to the inverting input of IC4/6. Approximately 39 % of the balance voltage then appears inverted at the

output of IC4/7. This voltage is inverted again, at unity gain, in IC6. Thus the balance voltage appears inverted at IC4/7, and non-inverted at IC6/1.

The tuning control voltage, applied also to IC4/6 inverting input appears at unity-gain inverted on IC4/7. The same control voltage is applied via R66 to IC6 inverting input, which is twice the current flowing through R57. Thus a unity-gain inverted replica of the tuning voltage appears at both IC4/7 and IC6/1.

10.3.8 VCA Law Shaping Circuits

The VCAs have a non-linear control characteristic, which in this application would result in the VCA control range being concentrated at one end of the available control range. The law shapers approximately linearise the VCA control characteristic. The input/output characteristic is shown in the graph, Figure 10.3.1, below. At an output voltage higher than -6 V approx., D17 conducts to halve the gain around IC4 for input voltages between -3 V and -10 V.

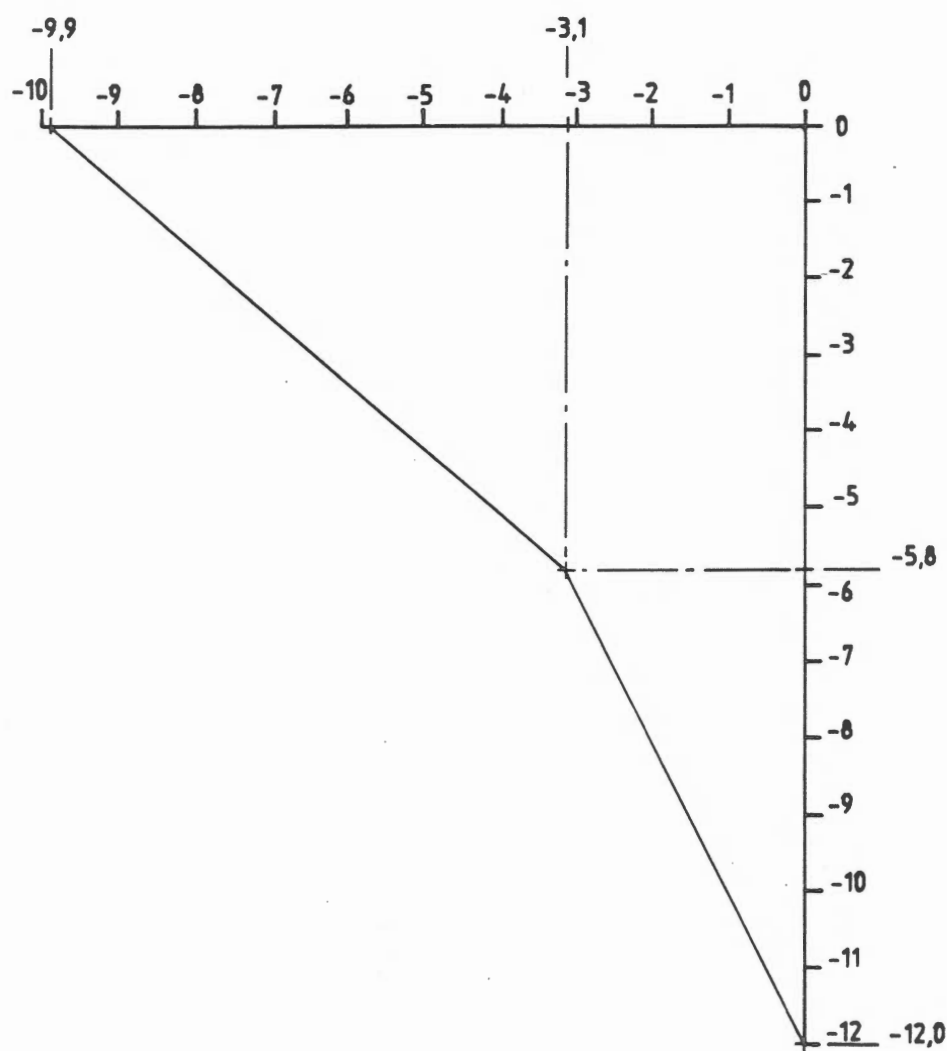


Figure 10.3.1 VCA Law Shaper Transfer Characteristic

10.3.9 Tuning Limit Comparators

Two of the four sections of IC10 are configured as comparators to signal to the microcomputer if the tuning voltage strays outside its normal operating range.

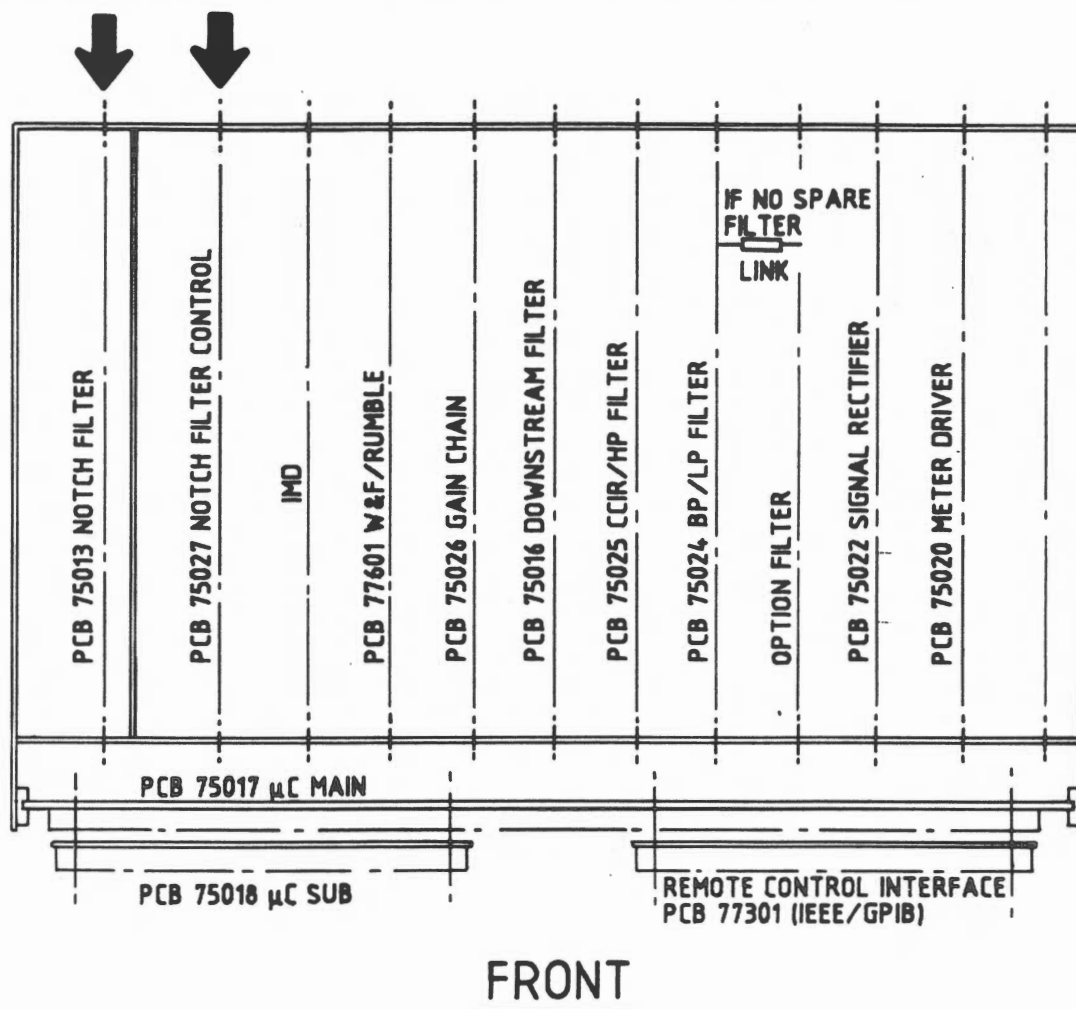
Pin IC10/1 goes high if the tuning voltage on IC7/7 exceeds 0 V. Conversely, pin IC10/2 goes high if the voltage on IC7/7 drops below -10 V.

10.4 Removal/Replacement

Switch off the MJS401D and remove the mains lead.

Remove the four screws retaining the top cover. Pull the cover straight up.

With the instrument facing you, the Notch Filter card is in the leftmost slot in the main card frame, in its own separate compartment. The Notch Filter Control card is in the adjacent slot, to the right of the Notch Filter.



MJS401D PCB Location Guide

Remove a card by grasping the top corners and gently pulling up.

Replacement is the opposite of removal. Carefully line up the connectors before pushing down and ensure the cards are properly held within the guides.

Extender cards PCB75028 (Notch Filter) and PCB75034 (Notch Filter Control) may be used to facilitate repair and recalibration.

10.5 Calibration

10.5.1 Notch Filter

There are no adjustments to be made on the notch filter card.

The following D.C. voltage measurements will help to establish basic functionality (use Extender Card PCB75028)

IC1	pin 6	0 $\pm$ 100 mV
IC9	pin 6	0 $\pm$ 100 mV
IC8	pin 6	0 $\pm$ 100 mV
IC11	pin 6	0 $\pm$ 100 mV
IC17	pin 6	0 $\pm$ 100 mV
D14	cathode	+4.5 V to +5.25 V
D5	cathode	+7.0 V to +8.0 V
D6	anode	-7.0 V to -8.0 V
D11	cathode	+7.0 V to +8.0 V
D12	anode	-7.0 V to -8.0 V
IC7	pin 4	-9 V to -11 V
IC18	pin 1	+4.5 V to +5.25 V

10.5.2 Notch Filter Control

Use Extender Card PCB75034. Check the following D.C. voltages:

D10	cathode	+3.2 V to +3.5 V
D11	anode	-3.2 V to -3.5 V
D13	cathode	+7.1 V to +7.9 V
D14	anode	-7.1 V to -7.9 V
D1	anode	-8.7 V to -9.6 V
D15	cathode	+5.9 V to +6.5 V
D2	cathode	+5.9 V to +6.5 V
D3	cathode	+5.9 V to +6.5 V
IC2	pin 2	-0.8 V to -2.2 V
IC2	pin 3	same as IC2 pin 2
IC2	pin 5	-7.9 V to -8.5 V
IC2	pin 6	+11 V to +15 V
IC2	pin 12	+11 V to +15 V
IC8	pin 2	-0.8 V to -2.2 V
IC8	pin 3	same as IC8 pin 2
IC8	pin 5	-7.9 V to -8.5 V
IC8	pin 6	+11 V to +15 V
IC8	pin 12	+11 V to +15 V
IC10	pin 8	+1.3 V to +1.4 V
IC10	pin 5	+2.2 V to +2.4 V
IC10	pin 6	+7.2 V to +8.2 V
IC3	pin 6	0 mV $\pm$ 20 mV
IC9	pin 6	0 mV $\pm$ 20 mV

Connect an oscilloscope to the 'SCOPE socket.

Apply the signal from a low distortion (<0.002 %) oscillator to Input A.

MD404B may be used if fitted by plugging a cable between the INPUT A and OSCILLATOR connectors. An oscillator of higher distortion than 0.002 % will not allow adjustment of the residual distortion.

MJS401D Front Panel Setup

Input	Load	Function	Filters	Rectifier	Scale	Dist'n	Coarse	Fine
A	Off	THD + N	30 kHz	RMS	% Dist	-80 dB	0	0

Sinewave Source Setup

Freq	Level		Source
	dBu	Volts	Impedance
220 Hz	+22	9.8	Low

If the oscillator in use will not reach +22 dBu, set it to +12 dBu (3.1 V) or +2 dBu (0.98 V) instead.

Adjust VR2 and VR3 for the lowest residual reading. Observe the 'scope trace to ensure that the waveform only consists of harmonics and a little random noise. There should be neither mains hum, periodic interference, nor very high levels of random noise.

Sinewave Source Setup

Freq	Level		Source
	dBu	Volts	Impedance
22 Hz	+22	9.8	Low

Adjust VR1 and VR4 for the lowest residual reading. The same remarks apply as for the previous paragraph. There is a noticeable delay between making the adjustment and seeing the full result, so do not try to adjust too quickly.

Repeat the above two steps until no further improvement can be made.

10.5.3 THD+N System

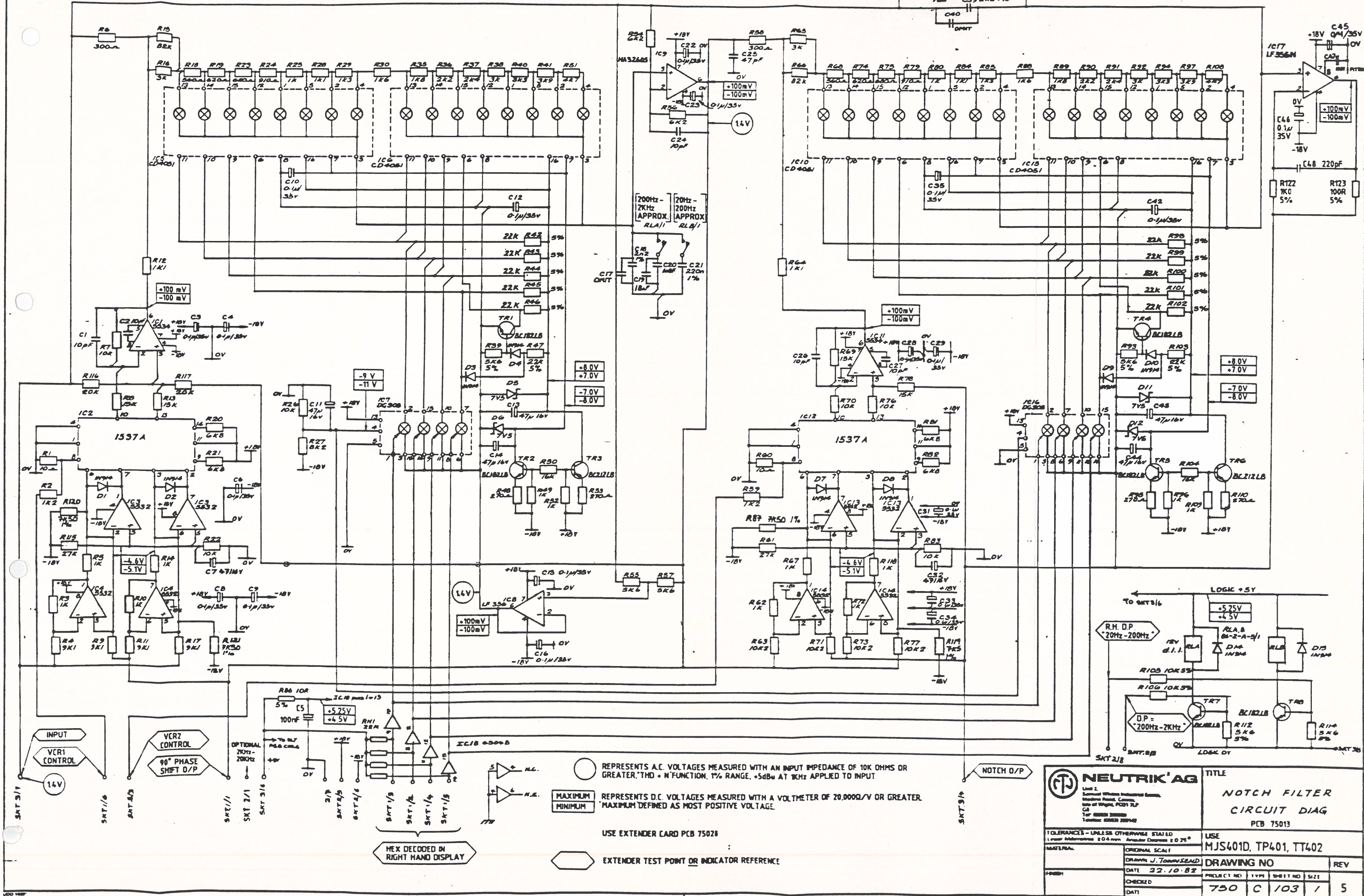
The remaining adjustments which affect THD+N measurements are on the Downstream Filter. See section 6 of this manual for calibration instructions.

PROJECTION DO NOT SCALE IF IN DOUBT ASK

ALL RESISTORS 1% UNLESS OTHERWISE STATED

HIGHEST	MISSING
R121 IC18	R31 RT11
R41 TR8	R32 RT13
C47 DT5	R33 DT13
SKT3 RLB	R34 C30
	R107 C41

REVISION		
NO	DATE	CHANGE
1	10/1/82	INITIAL DESIGN
2	10/1/82	REVISED TO MATCH PCB
3	10/1/82	REVISED TO MATCH PCB
4	10/1/82	REVISED TO MATCH PCB
5	10/1/82	REVISED TO MATCH PCB



REPRESENTS A.C. VOLTAGES MEASURED WITH AN INPUT IMPEDANCE OF 10K OHMS OR GREATER, THD = N/FUNCTION, 1% RANGE, +5dBm AT 1KHz APPLIED TO INPUT

REPRESENTS D.C. VOLTAGES MEASURED WITH A VOLTMETER OF 20,000Ω/V OR GREATER, MAXIMUM DEFINED AS MOST POSITIVE VOLTAGE

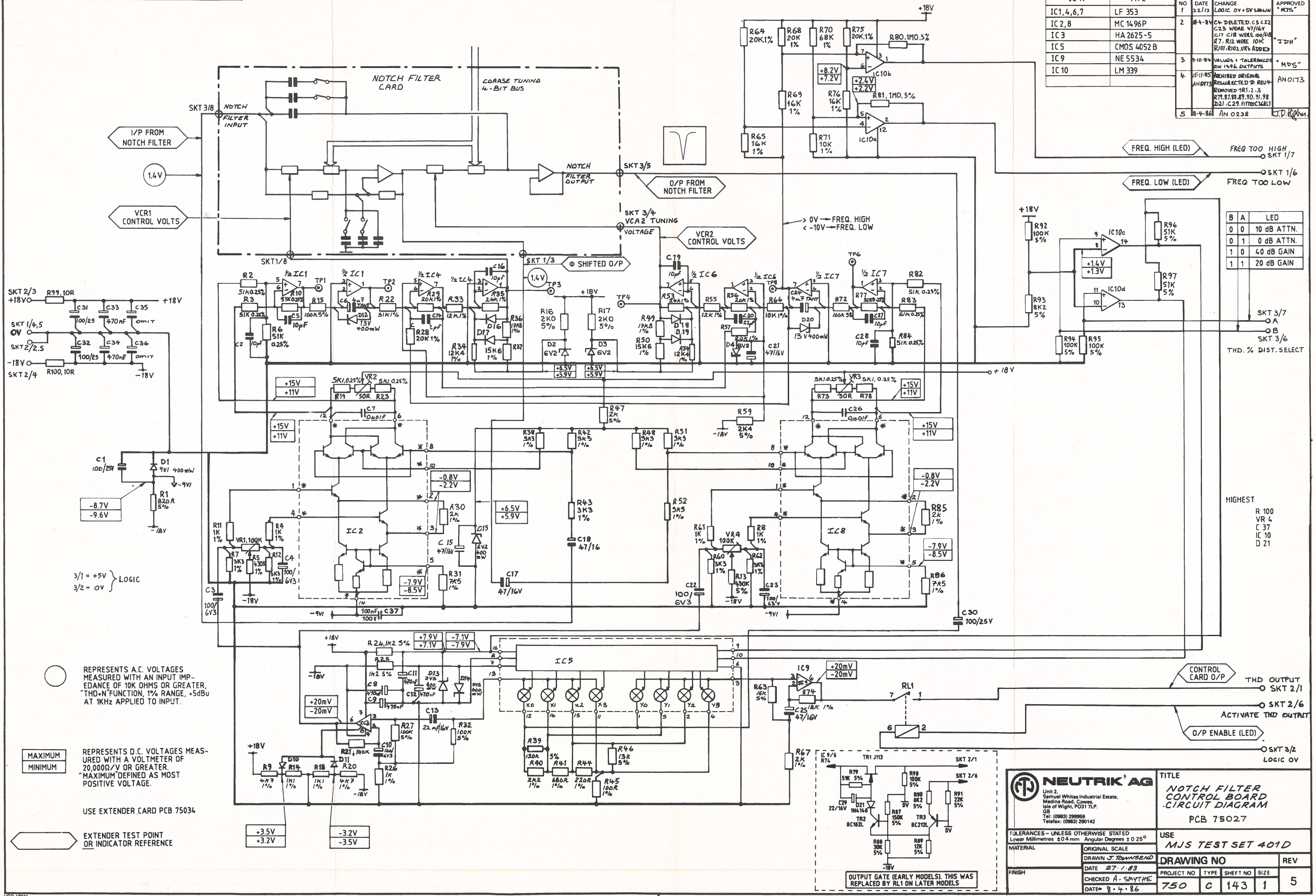
MAXIMUM MINIMUM

USE EXTENDER CARD PCB 75010

EXTENDER TEST POINT OR INDICATOR REFERENCE

NEUTRIK AG		TITLE	
Laser Lithography Division Munich, Germany Tel: 089 309000 Telex: 520942		NOTCH FILTER CIRCUIT DIAG PCB 75013	
TOLERANCES - UNLESS OTHERWISE STATED Resistors: 1% unless otherwise stated Capacitors: 5% unless otherwise stated		USE MJS401D, TP401, TT402	
ORIGINAL SCALE DATE 22.10.82 CHECKED DATE		DRAWING NO 750 C 103 1 5	

IC No		TYPE	REVISION		
IC 1, 4, 6, 7	LF 353		NO	DATE	CHANGE
IC 2, 8	MC 1496P		1	22/12	LOGIC OV + SV 500mV
IC 3	HA 2625-5		2	18-4-84	C4 DELETED, C3, C22, C23 WERE 47/16V, C17, C18 WERE 100/50V, R7, R12 WERE 10K, R101, R102, VR4 ADDED
IC 5	CMOS 4052B		3	9-10-84	VALUES + TOLERANCES ON 1496 OUTPUTS
IC 9	NE 5534		4	15-11-85	REMOVED ORIGINAL RESISTORS TO REV4, REMOVED TR1, 2, 3, R7, R8, R9, R10, R11, R12, C29, FITTED C40
IC 10	LM 339		5	18-4-86	AN 0238



3/1 = +5V } LOGIC
3/2 = 0V }

REPRESENTS A.C. VOLTAGES MEASURED WITH AN INPUT IMPEDANCE OF 10K OHMS OR GREATER, THD-N-FUNCTION, 1% RANGE, +5dBu AT 1KHz APPLIED TO INPUT.

REPRESENTS D.C. VOLTAGES MEASURED WITH A VOLTMETER OF 20,000Ω/V OR GREATER. *MAXIMUM DEFINED AS MOST POSITIVE VOLTAGE.

USE EXTENDER CARD PCB 75034

EXTENDER TEST POINT OR INDICATOR REFERENCE

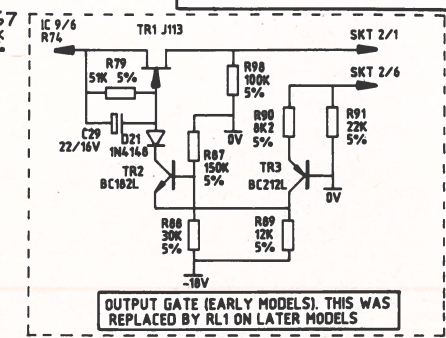
FREQ. HIGH (LED) FREQ TOO HIGH
FREQ. LOW (LED) FREQ TOO LOW

B	A	LED
0	0	10 dB ATTN.
0	1	0 dB ATTN.
1	0	40 dB GAIN
1	1	20 dB GAIN

SKT 3/7
SKT 3/6
THD. % DIST. SELECT

HIGHEST
R 100
VR 4
C 37
IC 10
D 21

CONTROL CARD O/P
THD OUTPUT
O/P ENABLE (LED)
LOGIC OV



Unit 2, Samuel Whites Industrial Estate, Medina Road, Cowes, Isle of Wight, PO31 7LP.
Tel: (0983) 299969
Telefax: (0983) 290142

TOLERANCES - UNLESS OTHERWISE STATED
Linear: Millimetres ±0.4mm Angular: Degrees ±0.25°

MATERIAL ORIGINAL SCALE
DATE 27.1.83
CHECKED A. SMYTHE
DATE 8.4.86

USE
MJS TEST SET 401D

DRAWING NO 750
PROJECT NO C
TYPE 143
SHEET NO 1
SIZE 1
REV 5